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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/965,286	11/06/1997	TAKAYUKI GOMI	P97.2608	3718

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 08/965,286	Applicant(s) GOMI ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,20-26,30 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,21-23,25,26,30 and 31* is/are rejected.

7)☒ Claim(s) *20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: Claim 1 recites the limitation "said transistors" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 4, 6, 21-23, 25-26 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (4,258,379).

Regarding claim 1, Watanabe et al. teach in figure 8 a semiconductor device having a first vertical bipolar transistor 101 and a second vertical type transistor 201 having a high breakdown voltage, the transistors each having an emitter, a base and a collector, the semiconductor device comprising a silicon substrate of a first conductivity P type 1,

an epitaxial layer 3 formed on the substrate, a first embedded diffusion layer 21 formed as a part of the first vertical bipolar transistor 101 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 22" formed as a part of the second vertical type transistor directly on the substrate in a second upper part of the substrate, wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer, and having opposite conductivity type as that of the substrate and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer and is approximately equal to or higher than the impurity concentration of the epitaxial layer (figure 9), wherein peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from a surface of the emitter of the first and second vertical type bipolar transistors such that the first distance is smaller than the second distance.

Watanabe et al. do not a state that the second vertical type transistor has a breakdown voltage that is higher than that of the first vertical type transistor. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second vertical type transistor having a breakdown voltage that is higher than that of the first vertical type transistor in Watanabe et al.'s device in order to use the device in an application which requires a second vertical type transistor having a higher

breakdown voltage than that of the first vertical type transistor. Note that a recitation which occurs in the preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 3, Watanabe et al. teach in figure 9 a bottom of the first embedded diffusion layer 21 being formed at a smaller distance from the surface of the emitter than the bottom of the second embedded diffusion layer 22".

Regarding claims 4 and 21, Watanabe et al. teach in figure 9 a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer.

Regarding claim 22, Watanabe et al. teach a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the surface of the emitter that is approximately equal to a location of the bottom of the first embedded diffusion layer from the surface of the emitter.

Regarding claim 23, Watanabe et al. teach a first vertical type bipolar transistor defining a voltage that is different than that of the second vertical type bipolar transistor, wherein the first embedded diffusion layer having an impurity concentration that is higher than that of the epitaxial layer.

Regarding claim 6, Watanabe et al. teach substantially the entire claimed structure, as applied to claim 6 above, except a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Watanabe et al.'s device, since it is within the skills of an artisan to form a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15, subject to routine experimentation and optimization. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed.

Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 26, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

Regarding claims 30 and 31, the first vertical type bipolar transistor is capable of operating at a higher speed and a lower voltage tan the second vertical type bipolar transistor.

Allowable Subject Matter

4. Claims 20 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

5. The following is an examiner's statement of reasons for allowance: Watanabe et al. (4,258,379) appear to be the closest prior art reference. Watanabe et al. teach substantially the entire claimed structure as recited in claim 1, except having

only the epitaxial layer being disposed between the base layer and the second embedded diffusion layer. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Response to Arguments

6. Applicant arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

Ori Nadav

December 4, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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